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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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John R. Thompson
STOEL RIVES LLP
One Utah Center, Suite 1100
201 South Main Street
Salt Lake City, UT 84111

EXAMINER	
DSOUZA, JOSEPH FRANCIS A	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 12/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,004	BOSE ET AL.	
	Examiner	Art Unit	
	Adolf DSouza	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 – 2, 4, 10, 11, 14, 15, 18, 19, 23, 24, 25, 28, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lian** (FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR filters, October 2000, IEEE Workshop on Signal Processing Systems, pages 317 – 325; which has been provided by the Applicant in his IDS) in view of **Lee et al.** (GA-Based Design of Multiplierless 2-D Digital Filters with very low roundoff noise, date, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, Nov 18 – 21, 1996, pages 223 – 226; which has been provided by the Applicant in his IDS).

Regarding claim 1, Lian discloses a multiplierless IIR digital filter, comprising:

a memory having stored thereon power-of-two coefficients (Fig.4, element “ROM”; page 321, 1st 3 lines; page 322, last 3 lines - page 323, 1st 2 lines);

a first-shift register having an input to receive input samples (Fig. 4, element dual port RAM; page 322, last 3 lines - page 323, 1st 2 lines; wherein the elements of Fig. 4 are used to implement the feed forward part of the IIR filter);

a second shift register having an input to receive previous outputs (Fig. 4, element dual port RAM; page 322, last 3 lines - page 323, 1st 2 lines; wherein the elements in Fig. 4 are used to implement the feedback part of the IIR filter, since as described Fig. 4 can be used to implement several subfilters);

a shifter stage in communication with the memory and the shift registers to receive the power-of-two coefficients, input samples, and previous outputs and perform a shift operation for corresponding power-of-two coefficients, input samples and previous outputs to thereby produce products (Fig. 4, elements "programmable shifters", ROM; page 322, last 3 lines - page 323, 1st 2 lines; wherein the memory is the ROM which stores the power-of-two coefficients);

and an adder stage, in communication with the shifter stage, to receive the products and provide a summation of the products (Fig. 4, element "adders"; page 322, last 3 lines - page 323, 1st 2 lines).

Lian does not disclose that the powers of two coefficients are derived from a genetic algorithm.

In the same field of endeavor, however, Lee discloses the powers of two coefficients are derived from a genetic algorithm (Abstract; page 224, section 3; page 226, section 5, 1st paragraph).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Lee, in the system of Lian because this would allow the use of multiplierless filters, thereby making them attractive for low cost implementation and high-speed operation, as disclosed by Lee (Abstract).

Regarding claim, 2 Lian discloses that the memory is a ROM (Fig. 4, element "ROM").

Regarding claim 4, Lian discloses that the shifter stage includes barrel shifters with each barrel shifter performing a shift operation for a received power-of-two coefficient (Fig. 4, element "programmable shifters"; page 322, last 3 lines - page 323, 1st 2 lines; wherein the barrel shifters are interpreted as the programmable shifters).

Regarding claim 10, Lian discloses a controller in communication with the memory and the shift registers (Fig. 4, element "control logic").

Claims 11, 18, 24 are directed to apparatus of the same subject matter claimed in method/steps claim 1 and therefore, are rejected as explained in the rejection of claim 1 above.

Claims 12, 26 are directed to apparatus of the same subject matter claimed in method/steps claim 1 and therefore, are rejected as explained in the rejection of some limitations of claim 1 above.

Claims 14, 19, 25 are directed to apparatus of the same subject matter claimed in method/steps claim 2 and therefore, are rejected as explained in the rejection of claim 2 above.

Claims 15, 28 are directed to apparatus of the same subject matter claimed in method/steps claim 4 and therefore, are rejected as explained in the rejection of claim 4 above.

Claims 23, 33 are directed to apparatus of the same subject matter claimed in method/steps claim 10 and therefore, are rejected as explained in the rejection of claim 10 above.

3. Claim 3, 13, 20, 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lian** (FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR filters, October 2000, IEEE Workshop on Signal Processing Systems, pages 317 – 325) in view of **Lee et al.** (GA-Based Design of Multiplierless 2-D Digital Filters with very low roundoff noise, date, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, Nov 18 – 21, 1996, pages 223 – 226) an further in view of **Butler et al.** (US 20020131487) and **Muhammad et al.** (US 20030083852).

Regarding claim 3, Lian does not disclose that a first multiplexer receives input samples form a shift register and a second multiplexer receives feedback samples from a shift register.

In the same field of endeavor, however, Butler discloses a first multiplexer in communication with the first shift register to receive the input samples (Fig. 1, input samples fed to shift register 20; Fig. 7, input vector S10 from the shift register fed to the multiplexers M10a, M10b, M20a, M20b).

In the same field of endeavor, however, Muhammad discloses a second multiplexer in communication with the second shift register to receive the previous outputs (Fig. 8b, elements 885, 886; page 12, paragraph 110; wherein the second multiplexer 886 selects one of the samples from the shift register 885 which receives the feedback samples).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the methods, as taught by Butler and Muhammad, in the system of Lian because this would allow the input and feedback samples to be selected by the multiplexers for multiplication by the appropriate filter coefficient, as is well known in the art.

Claims 13, 20, 27 are directed to apparatus of the same subject matter claimed in method/steps claim 3 and therefore, are rejected as explained in the rejection of claim 3 above.

4. Claim 5, 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Lian** (FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR filters, October 2000, IEEE Workshop on Signal Processing Systems, pages 317 – 325) in view of **Lee et al.** (GA-Based Design of Multiplierless 2-D Digital Filters with very low roundoff noise, date, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, Nov 18 – 21, 1996, pages 223 – 226) and further in view of **Yeum** (US 20020126858).

Regarding claim 5, Lian does not disclose the shifter stage includes 32 barrel shifters.

In the same field of endeavor, however, Yeum discloses the shifter stage includes 32 barrel shifters (page 2, paragraphs 24 and 33; Fig. 2, elements 451, 452, 453; wherein the 32 barrel shifters is interpreted as being encompassed by the plurality of barrel shifters).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Yeum, in the system of Lian because this would allow faster processing speed of the system, as disclosed by Yeum (page 2, paragraph 24).

Claims 21 is directed to apparatus of the same subject matter claimed in method/steps claim 5 and therefore, are rejected as explained in the rejection of claim 5 above.

5. Claims 6 – 9, 16, 17, 22, 29, 30, 31, 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Lian** (FPGA Implementation of High Speed Multiplierless Frequency Response Masking FIR filters, October 2000, IEEE Workshop on Signal Processing Systems, pages 317 – 325) in view of **Lee et al.** (GA-Based Design of Multiplierless 2-D Digital Filters with very low roundoff noise, date, Proceedings of IEEE Asia Pacific Conference on Circuits and Systems, Nov 18 – 21, 1996, pages 223 – 226) and further in view of **Shah et al.** (US 4,862,402).

Regarding claim 6, Lian does not disclose an adder tree having adder elements disposed in series.

In the same field of endeavor, however, Shah discloses the adder stage includes an adder tree having adder elements disposed in series (Fig. 3a; Abstract; column 3, lines 44 – 45; column 5, lines 35 - 42).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Shah, in the system of Lian because this would allow high frequency capability, as disclosed by Shah (Abstract).

Regarding claim 7, Lian does not disclose that each adder receives two inputs and provides a sum.

In the same field of endeavor, however, Shah discloses that each adder element includes an adder for receiving two values and providing a sum (Fig. 3a).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Shah, in the system of Lian because this would allow high frequency capability, as disclosed by Shah (Abstract).

Regarding claim 8, Lian does not disclose that two adder trees in parallel.

In the same field of endeavor, however, Shah discloses the adder stage includes two adder trees disposed parallel to one another to receive products from the shifter stage (Fig. 3a).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Shah, in the system of Lian because this would allow high frequency capability, as disclosed by Shah (Abstract).

All other elements of claim 8 are as analyzed in claims 6 and 7 above.

Regarding claim 9, Lian discloses an accumulator in communication with the adder stage to receive values from the adder stage and provide a sum of the values (Fig. 4, element “pipelined accumulator”).

Claims 22, 29 are directed to apparatus of the same subject matter claimed in method/steps claim 6 and therefore, are rejected as explained in the rejection of claim 6 above.

Regarding claim 16, Lian does not disclose adding the products in parallel includes disposing adder elements in series.

In the same field of endeavor, however, Shah discloses adding the products in parallel includes disposing adder elements in series, each adder element having an adder for receiving two values and providing a sum (Fig. 3; wherein adding products in parallel is done by the parallel adder trees).

Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Shah, in the system of Lian because this would allow high frequency capability, as disclosed by Shah (Abstract).

Claims 17, 32 are directed to apparatus of the same subject matter claimed in method/steps claim 9 and therefore, are rejected as explained in the rejection of claim 9 above.

Claims 30 - 31 are directed to apparatus of the same subject matter claimed in method/steps claims 7 - 8 and therefore, are rejected as explained in the rejection of claims 7 - 8 above.

Other Prior Art Cited

The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

The following patents are cited to further show the state of the art with respect to multiplierless filters:

Lin (US 5,287,299) discloses a method and apparatus for implementing a digital filter employing coefficients expressed as sums of 2 to an integer power.

Wilson et al. (US 6,313,773) discloses a multiplierless interpolator for a delta-sigma digital to analog converter.

Willson et al. (US 20020013798) discloses Low-power pulse-shaping digital filters using multiplierless filters.

Van Bavel et al. (US 5,541,864) discloses arithmetic-free digital interpolation filter architecture.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Adolf DSouza whose telephone number is 571-272-1043. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Adolf DSouza
Examiner
Art Unit 2611

AD

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER